a leaky, thermally conductive insulator material (LTCIM) layer disposed directly on the semiconductor substrate; and

a semiconductor layer disposed directly on the LTCIM layer,

wherein the LTCIM layer comprises at least one of doped amorphous silicon, undoped amorphous silicon and undoped porous silicon, and

wherein the LTCIM layer extends over an entire lateral dimension of the semiconductor substrate.

Marked-up versions of the amended claims appear in an Appendix A.

REMARKS

Following entry of this amendment claims 1-3, 5, 17-19 will be pending. Claims 4, 6-10 have been canceled without prejudice or disclaimer. Claims 1, 5, 17 and 18 have been amended. Claim 1 and 18 have been amended, inter alia, to include the features of canceled claims 9-10, i.e., the LTCIM of "undoped porous silicon" and "amorphous silicon", respectively. Additional support for the features can be found in the specification at page 4, lines 26-28 and page 6 lines 10-14, for example. Support for the doped and undoped "amorphous silicon" can be found in the specification at page 6, lines 15-25, for example. The Applicants have enclosed in an Appendix B a complete set of claims for the Examiner's convenience.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 102

Claims 1-5 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,424,009 issued to Ju ("Ju"). Claims 1-8 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2002/0096717 issued to Chu et al. ("Chu"). Claims 1-2, 4 and 8-9 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Japanese Patent No. JP 2001-148479 issued to Be ("Be"). Claims 17-19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No.

6,424,009 issued to Ju ("Ju"). Withdrawal of the rejection is respectively requested for at least the following reasons.

A. Ju

Amended claim 1 and amended claim 18, *intra alia*, include "wherein the LTCIM layer comprises at least one of **doped amorphous silicon, undoped amorphous silicon and undoped porous silicon**". Ju does not teach or suggest forming a LTCIM layer of **doped amorphous silicon, undoped amorphous silicon** or **undoped porous silicon**. Ju discloses a semiconductor-on-insulator (SOI) structure 10 having a **polysilicon** layer 14 disposed between a semiconductor substrate 12 and a semiconductor layer 13(see, for example, the abstract, Fig. 1).

Since Ju does not teach one or more of the features as claimed in amended claim 1 or amended claim 18, claims 1 and 18 and the claims that depend directly or indirectly from amended claims 1 and 18 are patentable over Ju for at least the reasons stated above.

B. Chu

Chu, like Ju above, does not teach or suggest forming a LTCIM layer of **doped amorphous silicon, undoped amorphous silicon** or **undoped porous silicon** as claimed in amended claim 1. Chu discloses a transferable device-containing layer 140 for silicon-on-insulator applications (see, for example, the abstract, Fig. 2 and page 3, pars. 0027, 0029 . Further, Chu discloses a seed wafer substrate 110 containing an at least partially crystalline porous release layer 120. The seed wafer 110 is separated from a "transferable" device layer 140, 140' or 140''. The "transferable" device layer is bonded to an insulating substrate before or after the seed wafer is separated. " The at least partially crystalline porous layer may incorporate at least one porous silicon germanium alloy layer alone or in combination with at least one porous Si layer." See, for example, the abstract.

That is, Chu discloses the partially crystalline porous layer 120 of the seed wafer 110

to include at least one porous silicon germanium alloy layer. This one porous silicon germanium alloy layer may also include a porous Si layer. However, Chu does not disclose or suggest forming a LTCIM layer of **doped amorphous silicon, undoped amorphous silicon** or **undoped porous silicon** as claimed in amended claim 1.

Since Chu does not teach one or more of the features as claimed in amended claim 1, claim 1 and the claims that depend directly or indirectly from amended claim 1 are patentable over Chu for at least the reasons stated above.

C. Be

Additionally, amended claim 1, *intra alia*, includes "wherein the LTCIM layer **extends over an entire lateral dimension** of the semiconductor substrate." Support for this feature can be found in Fig. 1, for example. In addition to the reasons explained above with regards to the material of the LTCIM, Be does not disclose or suggest a LTCIM that **extends over an entire lateral dimension** of the semiconductor substrate.

Be discloses a lower silicon substrate 21 and an upper silicon pattern 25a. The upper silicon pattern 25a is electrically isolated from the lower silicon substrate 21 by an isolation layer 33a buried in the hole of an inverted T-shape. A silicon layer or porous silicon layer 23b is formed **below the channel area**. The porous silicon layer 23b electrically and **partially** connects the lower silicon substrate 21 with the upper silicon pattern 25a.

Since Be does not teach or suggest one or more of the features as claimed in amended claim 1, claim 1 and the claims that depend directly or indirectly from amended claim 1 are patentable over Be for at least the reasons stated above.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 103

Claims 1-2, 4, 6-7 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Japanese Patent No. JP 63-288067 issued to Osada ("Osada") in view of U.S. Patent No. 5,773,151 issued to Begley et al. ("Begley"). Withdrawal of the rejection

is respectively requested for at least the following reasons.

Amended claim 1, *intra alia*, includes "wherein the LTCIM layer comprises at least one of **doped amorphous silicon, undoped amorphous silicon and undoped porous silicon**." Further, amended claim1 includes "wherein the LTCIM layer **extends over an entire lateral dimension** of the semiconductor substrate." Further still, claim 1 includes a "(LTCIM) layer disposed **directly** on the semiconductor substrate;" and "a semiconductor layer disposed **directly** on the LTCIM layer". Osada does not disclose or suggest forming a LTCIM layer of **doped amorphous silicon, undoped amorphous silicon** or **undoped porous silicon**. Further, Osada does not disclose or suggest a LTCIM that **extends over an entire lateral dimension** of the semiconductor substrate (see, for example, Fig. 2). Further still, Osada does not teach or disclose a LTCIM layer disposed **directly** on a semiconductor substrate; and a semiconductor layer disposed **directly** on the LTCIM layer. Osada discloses a polysilicon layer 3 shaped onto an **insulating substrate** 1.

Begley does not make up for the deficiencies of Osada. Begley teaches an insulating layer 18 disposed on the device layer 20. The insulating layer 18 is an oxide (see, for example, Col 3. lines 1-3). Thus, there would not be a motivation to combine the teachings of Osada with the teachings of Begley.

Therefore, since Osada alone or in combination with Begley does not teach or suggest one or more of the features as claimed in amended claim 1, claim 1 and the claims that depend directly or indirectly from amended claim 1 are patentable over Osada in view of Begley for at least the reasons stated above.

CONCLUSION

In light of the foregoing, it is respectfully submitted that the present application is in condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present invention.

Serial No. 09/879,724 Attorney Docket No. F0522

If there are any fees resulting from this communication, please charge same to our Deposit Account No. 18-0988; Our Order No. F0522 (AMDSP0414US).

Respectfully submitted,
RENNER, OTTO, BOISSELLE & SKLAR, LLP

Andrew Romero

Andrew Romero, Reg. No. 43,890

1621 Euclid Avenue, 19th Floor
Cleveland, Ohio 44115-2191
Telephone: (216) 621-1113
Facsimile: (216) 621-6165

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Serial No. 09/879,724 Attorney Docket No. F0522

APPENDIX A to
REPLY TO OFFICE ACTION DATED OCTOBER 7, 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicant: Dong-Hyuk Ju et al.

Serial No: 09/879,724

Filing Date: June 12, 2001

Art Unit: 2826

Examiner: Ahmed N. Sefer

Title: **LEAKY, THERMALLY CONDUCTIVE INSULATOR MATERIAL (LTCIM) IN SEMICONDUCTOR-ON-INSULATOR (SOI) STRUCTURE**

Below is a marked-up version of the amended portions of the present application. Added text is underlined and deleted text is bracketed and struck through (i.e., [~~example~~]).

1. (Twice Amended) A semiconductor-on-insulator (SOI) structure [~~having~~] comprising;

a semiconductor substrate;

a leaky, thermally conductive insulator material (LTCIM) layer disposed directly on the semiconductor substrate; [~~and~~]

a semiconductor layer disposed directly on the LTCIM layer; and

active regions defined in the semiconductor layer by isolation trenches and the LTCIM layer,

wherein the LTCIM layer comprises at least one of doped amorphous silicon, undoped amorphous silicon and undoped porous silicon, and

wherein the LTCIM layer extends over an entire lateral dimension of the semiconductor substrate.

5. (Amended) The SOI structure according to claim 4, wherein the [~~silicon~~] LTCIM layer preferably has a resistivity value 10 Ohms-cm or greater.

17. (Twice Amended) [~~A semiconductor on-insulator (SOI)~~] The SOI structure according to claim 18, further comprising [~~having~~]:

[~~a semiconductor substrate;~~

~~a leaky, thermally conductive material (LTCIM) layer disposed directly on the semiconductor substrate;~~

~~a semiconductor layer disposed directly on the (LTCIM) layer;~~]

a gate defining a channel interposed between a source and a drain formed within an active region of the SOI structure; and

the active region defined in the semiconductor layer by isolation trenches and the LTCIM layer.

18. (Amended) A semiconductor-on-insulator (SOI) structure [~~having~~] comprising;

a semiconductor substrate;

a leaky, thermally conductive insulator material (LTCIM) layer disposed directly on the semiconductor substrate; and

a semiconductor layer disposed directly on the LTCIM layer,

wherein the LTCIM layer comprises at least one of doped amorphous silicon, undoped amorphous silicon and undoped porous silicon, and

wherein the LTCIM layer extends over an entire lateral dimension of the semiconductor substrate.

Serial No. 09/879,724 Attorney Docket No. F0522

APPENDIX B – COMPLETE SET OF CLAIMS

In re patent application of:

Applicant: Dong-Hyuk Ju et al.

Serial No: 09/879,724

Filing Date: June 12, 2001

Art Unit: 2826

Examiner: Ahmed N. Sefer

Title: **LEAKY, THERMALLY CONDUCTIVE INSULATOR MATERIAL (LTCIM) IN SEMICONDUCTOR-ON-INSULATOR (SOI) STRUCTURE**

1. A semiconductor-on-insulator (SOI) structure comprising;

a semiconductor substrate;

a leaky, thermally conductive insulator material (LTCIM) layer disposed directly on the semiconductor substrate;

a semiconductor layer disposed directly on the LTCIM layer; and

active regions defined in the semiconductor layer by isolation trenches and the LTCIM layer,

wherein the LTCIM layer comprises at least one of doped amorphous silicon, undoped amorphous silicon and undoped porous silicon, and

wherein the LTCIM layer extends over an entire lateral dimension of the semiconductor substrate.

2. The SOI structure according to claim 1, wherein the semiconductor substrate material is silicon (Si), silicon carbide (SiC), silicon germanium (SiGe) or any other semiconductive material.

3. The SOI structure according to claim 1, wherein the LTCIM layer has a thermally conductivity value between about 30 W/mK to about 170 W/mK.

5. The SOI structure according to claim 4, wherein the LTCIM layer preferably has a resistivity value 10 Ohms-cm or greater.

17. The SOI structure according to claim 18, further comprising;

a gate defining a channel interposed between a source and a drain formed within an active region of the SOI structure; and

the active region defined in the semiconductor layer by isolation trenches and the LTCIM layer.

18. A semiconductor-on-insulator (SOI) structure comprising;

a semiconductor substrate;

a leaky, thermally conductive insulator material (LTCIM) layer disposed directly on the semiconductor substrate; and

a semiconductor layer disposed directly on the LTCIM layer,

wherein the LTCIM layer comprises at least one of doped amorphous silicon, undoped amorphous silicon and undoped porous silicon, and

wherein the LTCIM layer extends over an entire lateral dimension of the semiconductor substrate.

19. (Added) The SOI structure according to claim 18 further including;

a gate defining a channel interposed between a source and a drain formed within an active region of the SOI structure.